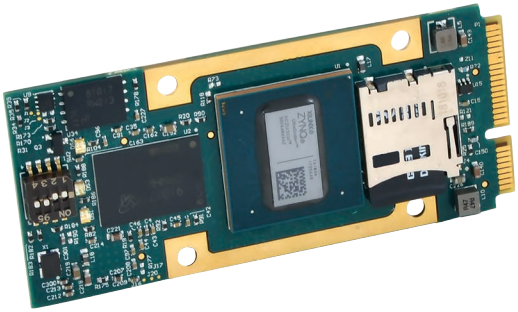
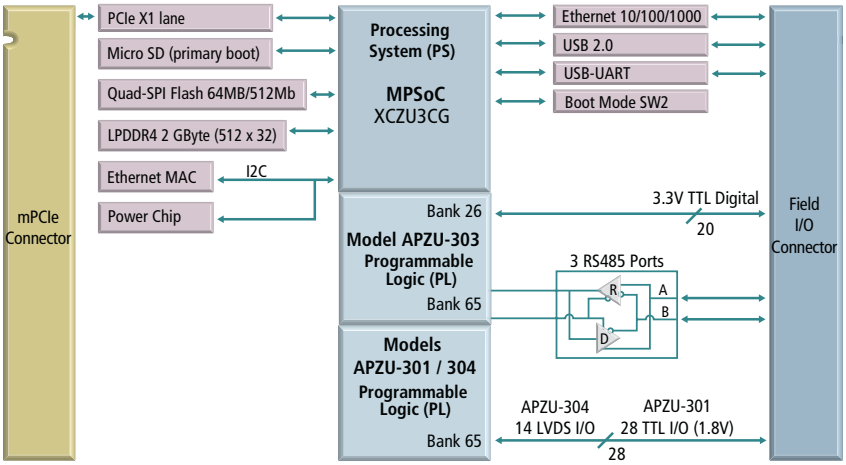
AcroPack® Modules

APZU Series User-Configurable Zynq® UltraScale+™ MPSoC I/O Modules

CE 2 YEAR WARRANTY RoHS Compliant





Xilinx® Zynq UltraScale+™ MPSoC ◆ ARM Cortex™ A53 & R5 CPUs ◆ Programmable logic ◆ PCIe Bus Interface

Models

APZU-301: 28 TTL I/O
APZU-303: 20 TTL and 3 RS485/422
APZU-304: 14 LVDS I/O

Description

AcroPack® modules are a ruggedized version of a mini PCIe card. AcroPacks add a down-facing 100-pin connector to internally route I/O signals through the carrier card to secure field connectors, thus eliminating loose cables and increasing reliability.

APZU series modules provide a programmable Xilinx Zynq UltraScale+ multiprocessor system on a chip (MPSoC). This MPSoC combines a feature-rich ARM-based processing system and programmable logic in a single device. Two dual-core ARM Cortex CPUs (A53 application processor and R5 real-time processor) deliver high-performance computation capability. Additional resources include on-chip memory, external memory interfaces, and a rich set of peripheral connectivity interfaces. The integrated ASIC-class programmable logic is ideal for compute-intensive tasks and offloading critical applications.

The real value of the Zynq UltraScale+ MPSoC architecture lies in the tight integration of its programmable logic with the processing system. Its high throughput interface eliminates bottlenecks that plague two-chip ASSP-FPGA solutions and allows designers to easily extend the processing system capabilities. Now developers can build custom designs by adding peripherals in the programmable logic and increase overall system performance by partitioning hardware and software functions with custom accelerators.

Designed for COTS applications these FPGA-based digital I/O modules deliver user-customizable I/O in a high-density and very rugged form factor. Typical applications involve adaptive filtering, sensor fusion, motor control, and image processing.

Acromag's Engineering Design Kit (EDK) provides an FPGA generated firmware example design that provides host access to the hardware digital I/O on the APZU module. The example is implemented using the Xilinx Vivado® development environment and offers a starting point from which customers can develop their customized applications.

Key Features & Benefits

Zynq MPSoC

- Dual-core ARM Cortex A53-based application processor unit (APU)
- Dual-core ARM Cortex R5-based real-time processor unit (RPU)
- NEON™ media-processing engine
- UltraScale+ 154k programmable logic cells
- Extensive on-chip memory

I/O and Peripherals

- TTL, LVDS, or RS422/485 I/O interface
- Gigabit Ethernet interface
- USB 2.0 transceiver
- USB-UART debug terminal port

General

- PCI Express interface
- MicroSD or NOR flash boot
- Quad-SPI flash memory
- LPDDR4 storage memory
- DMA transfers
- BSP and FPGA design kit software
- VxWorks®, Linux®, and Windows® support

Acromag® THE LEADER IN INDUSTRIAL I/O

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AcroPack® Modules

ISO9001
AS9100
MADE IN USA

Performance Specifications

Multiprocessor SoC

MPSoC device
Xilinx Zynq XCZU3CG-2SBVA484I.

Application processor: Dual-core ARM Cortex-A53, 1.3GHz. Single/double precision floating point unit.

Real-time processor: Dual-core ARM Cortex-R5, 533MHz. Single/double precision floating point unit.

NEON Advanced SIMD media-processing engine.

Programmable logic resources:
154,350 logic cells; 70,560 LUTs; 360 DSP slices.

Configuration
Primary boot from SD card or NOR flash alternate.

I/O and Peripheral Interfaces

I/O connector
68 pin field I/O (to carrier card).

Digital I/O
APZU-301: 28 TTL I/O channels (1.8V).
APZU-303: 20 TTL and 3 RS485/422 channels (3.3V).
APZU-304: 14 LVDS I/O channels.

Interrupts
20 channels of interrupts configurable for high-to-low, low-to-high, and change-of-state event types.

LPDDR Memory
2 Gbyte (512Mbit x 32).

Quad-SPI flash
512 Mbit (64 Mbyte) Nor flash device.

SD card interface
16 GB industrial MLC microSD card pre-programmed with boot.bin file.

Gigabit Ethernet interface
Supports 1000BASE-T, 100BASE-TX, and 10BASE-T. Zynq gigabit Ethernet controller uses a media independent interface (RGMII). External magnetics and RJ45 are provided on the breakout panel.

USB 2.0 interface
Microchip USB3320C.

UART to USB interface
Silicon Labs CP2103GM.

Breakout panel
Model 5028-626 panel mates directly to all 68-pin AcroPack carriers. Brings RJ45 ethernet port, USB 2.0 port, UART to USB port, digital I/O at jumper blocks, and power and reset buttons out to the field.

PCI Express

Compatibility
Conforms to PCI Express Base Specification, Rev.2.1.

PCIe interface
PCIe bus 1-lane (x1) Gen 1 interface.
2.5 Gbps signaling rate.

Memory space
1M Byte: BAR0 to Zynq DMA registers.
32K Byte: BAR1 to programmable logic register space.
64K Byte: BAR2 to DDR memory space.

Environmental

Operating temperature
Air-cooled (with heat spreader): -40 to 70°C (minimum airflow of 400LFM is recommended).
Conduction-cooled: -40 to 80°C.

Storage temperature
-55 to 125°C .

Relative humidity
5 to 95% non-condensing.

Power
3.3V DC (±5%): 57 mA typical, 100 mA max.
5.0V DC (±5%): 183 mA typical, 230 mA max.
+12V DC (±5%): 165 mA typical, 200 mA max.
1.5V, –12V DC: not used.

Vibration, sinusoidal operating
Designed to comply with IEC 60068-2-6.
10-500Hz, 5G, 2 hours/axis.

Vibration, random operating
Designed to comply with IEC 60068-2-64.
10-500Hz, 5G-rms, 2 hours/axis.

Shock, operating
Designed to comply with IEC 60068-2-27.
30G, 11ms half sine; 50G, 3mS half sine;
18 shocks at 6 orientations for both test levels.

Mean time between failure (MTBF)
MIL-HDBK-217F, FN2. Ground benign, controlled.

25°C: 1,459,102 MTBF hours; 167 MTBF years; 685.4 failure rate (FIT).

40°C: 923,762 MTBF hours; 105.5 MTBF years; 1,082.5 failure rate (FIT).

FIT is failures in 10^9 hours.

Physical

Dimensions
Length, width, height: 70 x 30 x 12.5 mm.
Board thickness: 1.0 mm.
Weight: 35.18 g (including heat spreader).

Engineering Design Kit

Board support package and FPGA design kit for Xilinx Vivado®. Example of IP Block design, block RAM, system monitor, AXI interface to digital I/O.

Kit must be ordered with the first purchase of an APZU module (see www.acromag.com for more information).

Ordering Information

AcroPack® Modules

Go to website product page for more information.

APZU-301
28 TTL channels (1.8V).

APZU-301-QSP
Quick Start Package includes APZU-301E-LF module, APCe7012 carrier, 5028-626 I/O panel, APZU-EDK software.

APZU-303
20 TTL & 3 EIA-485/422 channels (3.3V).

APZU-304
14 LVDS channels.

Accessories

APZU-EDK
Engineering design kit. (One kit required)

5028-626
I/O breakout panel with cables for Ethernet, USB, UART, JTAG, and 68-pin carrier card connections.

Carrier Cards

See Acromag.com/AcroPack-Carriers for a full list of AcroPack carrier cards.

Software

(see software documentation for details)

APSW-API-VXW
VxWorks® software support package.

APSW-API-WIN
Windows® DLL driver software support package.

APSW-API-LNX
Linux® support (website download only).

APZU-30x with included heat spreader attached