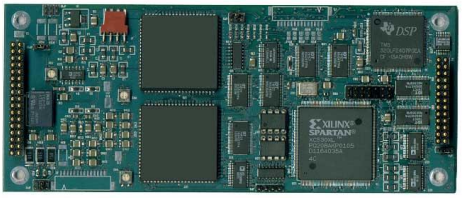
LUMISTAR

LS-40-P PCI Bit Synchronizer

Data Sheet

Description:

The Lumistar LS-40-P PCI Bit Synchronizer provides optimal reconstruction of a serial PCM data stream that has been corrupted by noise, phase jitter, amplitude modulation, or base line variations. The all-digital design assures a consistent product with high reliability and long-term stability. ***The LS-40-P PCI Bit Synchronizer consists of the LS-40-DB Bit Synchronizer Daughterboard shown below mounted on a PCI carrier board.***



A unique Built-in-Test feature allows performance verification modes for Bit Synchronizer. ***Auto-test BIT*** **is performed for a short duration on the application of power and tests 90% of the Bit Synchronizer components. This test verifies that power is properly applied, measures internal bit error rate, and performs other tests to ensure that the bit synchronizer is fully operational.** ***Command-test BIT*** **performs the same functions and can be commanded by the user at any time. Bit Sync also contains a BER reader as wall as frame sync pattern indicator.**

Key Features:

- **Up to 25 Mbps for NRZ-L (12.5 Mbps for Bi-Phase/Miller) PCM data codes**
- **Performance within 1 dB of theoretical to 10 Mbps (1.5 dB to 20 Mbps)**
- **All Digital Design ensures high reliability and long term performance**
- **Low power consumption**
- **Built-in-Test allows internal auto-test or command-test BER measurement**
- **Software selectable input 1 of 7**

Applicable Models:

LS-40-P25	**25 Mbps PCI Bit Synchronizer**
LS-40-P20	**20 Mbps PCI Bit Synchronizer**
LS-40-P10	**10 Mbps PCI Bit Synchronizer**

PCM Data Rate and Input Codes:

The LS-40-P Bit Synchronizers can operate over a range of 100 bits per second to their maximum data rates for all NRZ codes, or from 100 bits per second to half their maximum data rate for the Bi-Phase and Miller codes.

NRZ codes:	NRZ-L, NRZ-M, NRZ-S
RZ codes	RZ
Split phase codes	BIϕ-L, BIϕ-M, BIϕ-S
Miller codes	DM-M, DM-S, M^2-M, M^2-S
Randomized codes	RNRZ-L, RNRZ-M, RNRZ-S
Randomization sequence:	2^{11}-1, 2^{15}-1, 2^{17}-1, 2^{23}-1

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Input and Signal Characteristics:

Inputs signals:	Single-ended or differential
Input Impedance:	Shipped with 75Ω, 50Ω, 1KΩ (Jumper Select)
Input Polarity:	Auto-detect (normal or inverted)
Input Signal Amplitude:	0.4 V pp to 10 V pp
Maximum Voltage Input:	5V RMS for 50Ω and 75Ω Inputs 25V RMS for 1KΩ Impedance
Maximum DC Offset:	+/- 5V for 50Ω and 75Ω Inputs; +/- 25 V for 1KΩ Impedance
Dynamic AC baseline:	Baseline variations up to 100% of the input signal at rates to 0.1% of the signal frequency for sinewave or sawtooth signals (100 Hz max)

Phase-Locked Loop Performance:

Loop-Bandwidth:	Programmable from 0.01% to 2% depending on the Bit Rate of the input signal.
Acquisition Range:	0.04% to 8% depending on the Loop-Bandwidth selected
Tracking Range:	0.1% to 20% depending on the Loop-Bandwidth selected

Bit Error Rate Performance:

The LS-40 Bit Synchronizer performance relative to theoretical is indicated below when the applied signal has a S/N ratio within 1dB of the specified synchronization threshold with a Gaussian white noise bandwidth up to three times the bit rate, and has no jitter or base line variations on the input signal.

Codes:	Bit Rate:	Degradation from Theory:
NRZ	<10 Mbps	< 1 dB max (0.5 dB typical)
NRZ	10 to 25 Mbps	< 1.5 dB max (1 dB typical)
BIϕ, RZ	<5 Mbps	< 1 dB max (0.5 dB typical)
BIϕ, RZ	5 to 10 Mbps	< 1.5 dB max (1 dB typical)
DM, M^2	up to 10 Mbps	< 2 dB max (1 dB typical)

Capture Threshold:

The Capture Threshold when the applied signal has a S/N ratio within 1 dB of the specified synchronization threshold, has a Gaussian white noise up to three times the bit rate, and has no jitter or base line variations on the input signal is defined below:

Codes:	Capture Threshold:
NRZ	-1 dB (-3 dB typical)
BIϕ	+1 dB (+0 dB typical)

Synchronization Hold:

The LS-40 Bit Synchronizer is capable of maintaining synchronization during periods of signal loss or during continuous periods of 1s or 0s lasting up to 245 bits in every 1024 bits, for NRZ coded signals up to 5 Mbps or BIϕ coded signals up to 2.5 Mbps, providing:

- S/N ratio is greater than 12 dB
- PLL bandwidth is equal to 0.1%
- 50% Transition Density when the signal is present
- Input signal has no jitter or base line variations
- Signal has a constant amplitude

Acquisition Time:

The mean acquisition time is a function of the Loop Bandwidth and will be less than 100 bits with a Loop Bandwidth of 1% and less than 150 bits with a Loop Bandwidth of 0.1% for NRZ signals up to 5 Mbps or BIϕ signals up to 2.5 Mbps, providing:

- Gaussian white noise in a band up to three times the bit rate
- Transition Density is greater than 2% of the bit rate
- Signal has no jitter or baseline variations on the input signal

Output Signals:

Data	TTL and RS-422 Driven
Zero Degree Clock	TTL and RS-422 Driven
Tape Outputs	1 V pp into 50 Ω (code programmable) TTL and RS-422
Lock Status	In Status Register
Es/No >5dB Status	In Status Register
Input Signal Level Status	In Status Register
Built-in-test	In Status Register
Auxiliary Outputs/Inputs (Consult Lumistar for use)	3 Open ground inputs 4 Open ground outputs

Environmental:

Temperature (Operating)	0 to 50 ºC
Temperature (Non-Op)	-25 to +70 ºC
Humidity (Operating)	10% to 90% Non-Condensing

Physical:

Form Factor	Full size PCI board
Power required (typical)	6.5 W total @ max data rate 800ma @ +5V (typical), 10ma @ +12V (typical), 200ma @ -12V (typical)