LUMISTAR

LS-45-DB Dual Bit Synchronizer Daughterboard

Data Sheet

Description:

The Lumistar LS-45-DB Dual Channel Bit Synchronizer Daughterboard provides optimal reconstruction of a serial PCM data stream that has been corrupted by noise, phase jitter, amplitude modulation, or base line variations. The all-digital design assures a high performance, consistent product, with excellent reliability and long-term stability. Dual channel design can feed each channel of the LS-55-DD dual decom. The LS-45-DB also has a post D combiner that allows for optimal ratio combining of the two input signals

A unique Built-in-Test feature allows performance verification for the Bit Synchronizer to ensure the highest level of operation. *Auto-test BIT* is performed for a short duration on the application of power and tests more than 90% of the Bit Synchronizer components. This test verifies that power is properly applied, verifies that there are no internal bit errors, and performs other tests to ensure that the bit synchronizer is fully operational with status indication of results. *Command-test BIT* performs the same functions and can be initiated by the user at any time through the Lumistar software when used on Lumistar PC products. The user has the ability to generate internal pseudo-random patterns and calculate internal bit error rates with or without the injection of forced errors. Various status indicators are also available through the software. The Bit Synchronizer also contains a BER reader as well as frame sync pattern indicator.

Key Features:

- **PCM Data Rates up to 45 Mbps for NRZ-L (22 Mbps for Bi-Phase/Miller)**
- **Performance within 1 dB of theoretical to 20 Mbps (2 dB to 45 Mbps)**
- **All Digital Design ensures high reliability and long term performance**
- **2 single ended and 1 differential input per channel along with RX BERT reader.**
- **Low power consumption less than 8 watts.**
- **Built-in-Test with internal BER measurement and FSP reader**
- **Viterbi decoding for rate ½ k=7 (Other available consult factory)**

The Bit Synchronizer Daughter-boards can be installed on the LS-50-P PCI Multifunction PCM Decom, LS-55 Dual Channel PCI Multi-function Decom, LS-50-2Pe PCIe multi-function decom, LS-50-V VME Multifunction Decom, or the LS-22-SE Spectral and Oscilloscope Display. The Bit Synchronizer Daughter-boards are available on a PCI carrier (LS-45-P) or VME carrier (LS-45-V). The Lumistar LS-44-QBS incorporates 2 of the LS-45 Bit Synchronizer Daughter-boards in a 1U high rackmount chassis.

PCM Data Rate and Input Codes:

The LS-45-DB Bit Synchronizers can operate over a range of 100 bits per second to their maximum data rates for all NRZ codes, or from 100 bits per second to half their maximum data rate for the Bi-Phase and Miller codes.

NRZ codes:	NRZ-L, NRZ-M, NRZ-S	RZ codes	RZ
Split phase codes	BIϕ-L, BIϕ-M, BIϕ-S	Miller codes	DM-M, DM-S, M^2-M, M^2-S
Randomized codes	RNRZ-L, RNRZ-M, RNRZ-S	Randomization sequence:	2^{11}-1, 2^{15}-1, 2^{17}-1, 2^{23}-1

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Input and Signal Characteristics:

Inputs signals:	Single-ended or differential
No. of inputs	Up to 4 and internal simulator
Input Impedance:	Shipped with 75Ω, 50Ω, 1KΩ (Jumper Select)
Input Polarity:	Auto-detect (normal or inverted)
Input Signal Amplitude:	0.1 V pp to 10 V pp (nominal)
Maximum Voltage Input:	5V RMS for 50Ω and 75Ω Inputs 25V RMS for 1KΩ Impedance
Maximum DC Offset:	± 5V for 50Ω and 75Ω Inputs; ± 25 V for 1KΩ Impedance
Dynamic AC baseline:	Baseline variations up to 100% of the input signal at rates to 0.1% of the signal frequency for sinewave or sawtooth signals (100 Hz max)
De-randomizer	9, 11, 15 bit both forward and reverse

Phase-Locked Loop Performance:

Loop-Bandwidth:	Programmable from 0.001% to 5% depending on the Bit Rate
Acquisition Range:	0.04% to 8% depending on the Loop-Bandwidth selected
Tracking Range:	0.1% to 20% depending on the Loop-Bandwidth selected

Bit Error Rate Performance:

The LS-45 Bit Synchronizer performance relative to theoretical is indicated below when the applied signal has a S/N ratio within 1dB of the specified synchronization threshold with a Gaussian white noise bandwidth up to three times the bit rate, and has no jitter or base line variations on the input signal.

Codes:	Bit Rate:	Degradation from Theory:
NRZ	<20 Mbps	< 1 dB max (0.5 dB typical)
NRZ	20 to 30 Mbps	< 1.5 dB max (1 dB typical)
BIϕ, RZ	<10 Mbps	< 1 dB max (0.5 dB typical)
BIϕ, RZ	10 to 15 Mbps	< 1.5 dB max (1 dB typical)
DM, M^2	up to 15 Mbps	< 2 dB max (1 dB typical)

Capture Threshold:

The Capture Threshold when the applied signal has a S/N ratio within 1 dB of the specified synchronization threshold, has a Gaussian white noise up to three times the bit rate, and has no jitter or base line variations on the input signal is defined below:

Codes:	Capture Threshold:
NRZ	-1 dB (-3 dB typical)
BIϕ	+1 dB (+0 dB typical)

The capture range of the bit sync is up to ± 5% of the bit rate

Synchronization Hold:

The LS-45 Bit Synchronizer is capable of maintaining synchronization during periods of signal loss or during continuous periods of 1s or 0s lasting up to 245 bits in every 1024 bits, for NRZ coded signals up to 5 Mbps or BIϕ coded signals up to 2.5 Mbps, providing:

- S/N ratio is greater than 12 dB
- PLL bandwidth is equal to 0.1%
- 50% Transition Density when the signal is present
- Input signal has no jitter or base line variations
- Signal has a constant amplitude

Acquisition Time:

The mean acquisition time is a function of the Loop Bandwidth and will be less than 100 bits with a Loop Bandwidth of 1% and less than 150 bits with a Loop Bandwidth of 0.1% for NRZ signals up to 5 Mbps or BIϕ signals up to 2.5 Mbps, providing:

- Gaussian white noise in a band up to three times the bit rate
- Transition Density is greater than 2% of the bit rate
- Signal has no jitter or baseline variations on the input signal

Viterbi Decoding (Optional):

Rates	1/2, 2/3, 3/4, 5/6, 7/8
Constraint Length	k=7
Puncture Matrix	Per NASA Standards

Output Signals:

Data	TTL and RS-422 Driven
Clock	TTL and RS-422 Driven 0°, 90°, 180°, 270°
Tape Outputs	1 V pp into 50 Ω (code programmable) TTL and RS-422
Lock Status	In Status Register
Es/No >5dB Status	In Status Register
Input Signal Level Status	In Status Register
Built-in-test	In Status Register
Auxiliary Outputs/Inputs (Consult Lumistar for use)	3 Open ground inputs 4 Open ground outputs

Environmental:

Temperature (Operating)	0 to 50 ºC
Temperature (Non-Op)	-25 to +70 ºC
Humidity (Operating)	10% to 90% Non-Condensing

Physical:

Daughterboard for LS-50 Series
8 W total power 6.5” x 2.75”