Lumistar LS-48-R1 Series Dual Channel Bit Synchronizer

Single / Dual Bit Synchronization

Frame Synchronization

Bit Error Rate Detection
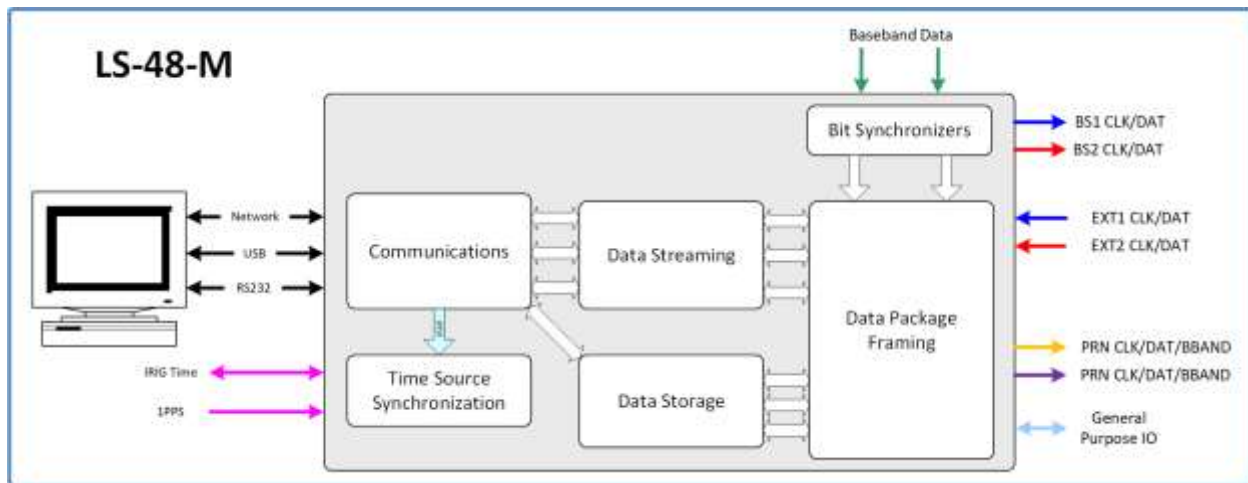
OPTIONS:

Telemetry over IP (TMoIP)

Data Recording

PRN Data Simulation

IRIG Time Code Reader/Gen

PTP Network Time Reader

Modular/Portable Versions

Rear Panel View

LS-48-R1 Series Products

LS-48-R1 Specifications:

- The LS-48-M Bit Sync is a child design, based upon the powerful LS-68-M "DPE" (Digital Processing Engine) baseband telemetry processing system. Some functions / capabilities installed in the LS-68-M are removed to produce the capabilities within the LS-48-M design.
- LS-48 is available in Modular, Portable and rack Mount configurations
- Ground, Mobile, Airborne/Shipboard & Remote Ops
- Flexible/Extensible Firmware-Based Personalities
- Single or Dual Channel Bit Synchronization available
- Single or Dual Frame Sync available
- Data Recording *(Optional)*
  - 64 GB per data channel (two channels each, internally stored)
  - > 7 hours per channel at 20 Mbps
- PRN Generation Capability
  - PRN Simulation
  - Real-time Network Streams
  - Maximum 2 PRN Streams per unit
- User Defined I/O Signals
- TTL and Differential High Speed 422 I/O
- Bit Error Rate Readers
- O-Scope Displays for Bit Synchronizer Input Visualization
- Viterbi Decoding available for Bit Sync Input Channels *(Optional)*
- No Commercial Internal OS
  - Control / Status over Ethernet, USB and RS-232
  - User Friendly Lumistar App Provided or Use Your Own
  - Compatible with IADS
- IRIG Time Code Reader and Generator Capability *(Optional)*
- IEEE-1588 Precision Time Protocol (PTP) Reader *(Optional)*
- Modular Unit Form Factor (inside the chassis)
  - 4.0" x 6.0" x 1.13"
  - Approx. 1.1 pounds
- AC Power
  - 110 – 240 VAC ; 47-63 Hz
  - 40 watts power dissipation *(Typical)*
- *For more technical information on the LS-48-M Series Products, please refer to the appropriate sections of the User Manual for the LS-68/48 Digital Processing Engine (DPE)*
  - *https://lumi-star.com/uploads/MANUALS/LS-68-M/LS-68-M_UserManual.pdf*

Lumistar, Inc   3186 Lionshead Ave. Suite 100   Carlsbad, CA 92010
Phone: 760-431-2181   FAX: 760-431-2665
Web: www.lumistar.net   September 2021   Email: sales@lumistar.net

BLOCK DIAGRAM
LS-48-M Series Bit Synchronizer

Some of the primary design objectives of the DPE product line were to reduce the platform size, to provide an "OS-less" environment by eliminating product use of commercial software operating systems for functional processing, to provide easy and flexible field upgrade/enhancements capabilities, and to provide a network appliance for device control and data transport. The unit is controlled and monitored using a 1000/100/10Mbps Ethernet interface with alternate controls being provided by USB and RS-232. Using provided documentation; the customer can develop their own interface GUI, or chose to utilize the provided Lumistar network application.

At the heart of the modular design is a flexible and extensible multi-core DSP Engine that can take on up to twelve "personalities". The device construction is via two hardware "slices": Signal Processing and a Control Processing Engine. Operational firmware loads, or "personalities", are retained internal to the device for quick switching between operational requirements. New firmware personalities and/or control processing revisions are easily updated in the field. No need to return the unit for most modifications.

Listed below are the specifications of the LS-48-M modular unit. If purchased as a Portable of 1U Rack Mount version, the Modular unit is installed in the package or chassis and all IO/Power/Ethernet are internally wired to the external faceplate.
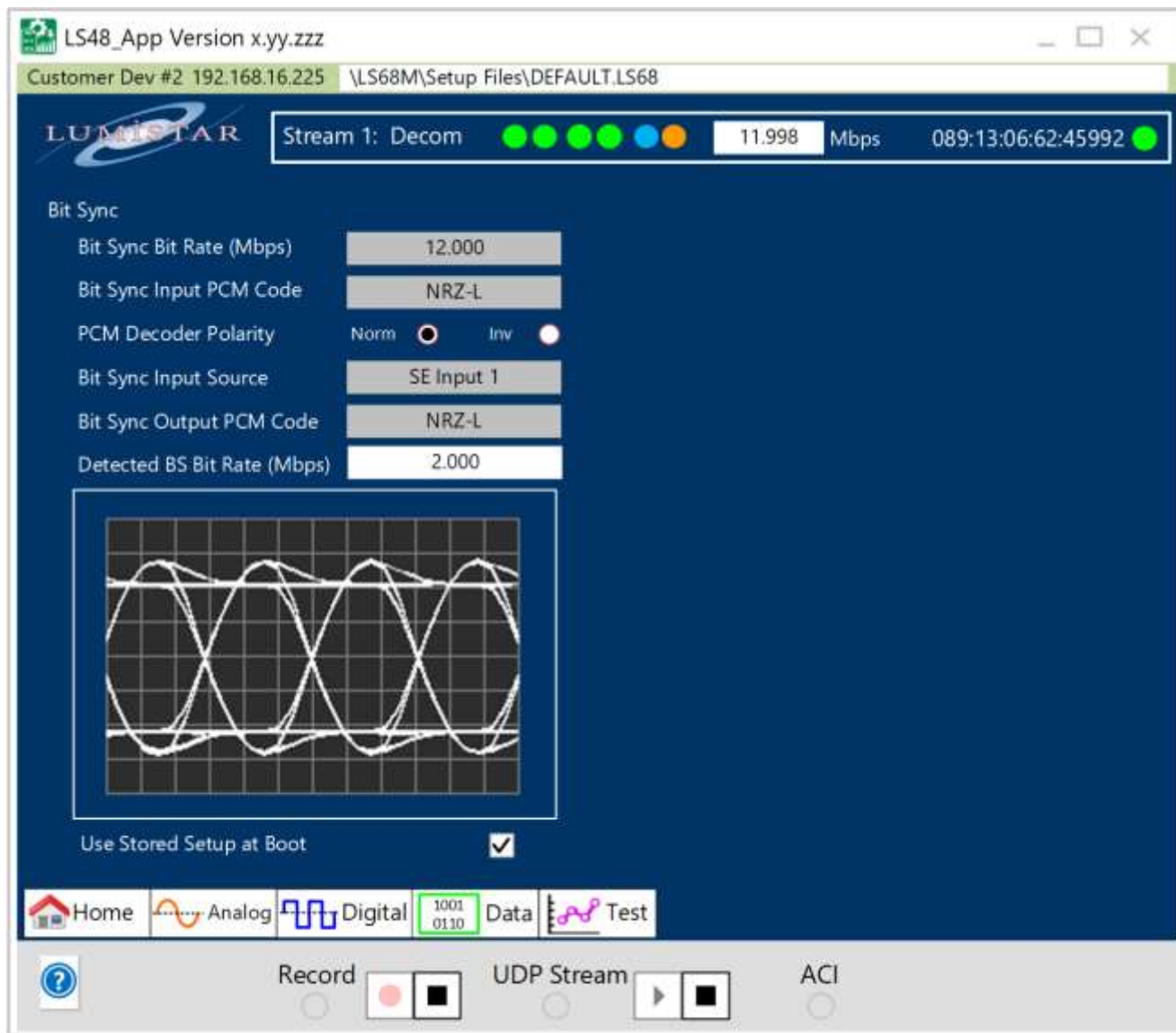
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General Specifications of the LS-48-M Modular Unit

Category:	Specifications:	Details:
Mechanical		
	Envelope Dimensions (all slices)	6.00"(L) x 4.00"(W) x 1.11" (H)
	Form Factor	Modular Brick
	Weight	~ 20oz.
Electrical		
	Individual power requirements	9-42VDC; Nom. +24VDC @ 0.875A
	Total Power (all streams)	~ 22 Watts (mode and data rate dependent)
Performance		
	1 or 2 PCM Bit Synchronizer	1kbps to 45Mbps (NRZ)
	1 or 2 PRN PCM Generators	PRN Pattern Generators; 1 per PCM Synchronizer
	PRN Baseband Output	15 Pre-mod filters; Variable output Voltage
	IRIG Time	A, B G; Generator and Reader
	Precision Time Protocol (PTP)	IEEE-1588
	Data Sources	TTL, Diff, Int. Bit Sync, Int. PRN
	Frame Data Size	16 bits; not user selectable
	Data Packaging Framing	3 to 65536 data frames
	Bit Sync Inputs	Single-Ended 1 and 2; Differential; SIM
	Data Recording/Playback FLASH	Available per channel; 64GB each (optional)
	Data Streaming	Raw or Throughput Modes Only
Connectors		
	Digital I/O Connector	(3) MicroDSub-25 Plug
	Power/Digital I/O Connector	(1) MicroDSub-25 Receptacle
Environmental		
	Temperature, Op	-40 to 85 C (Industrial)
	Temperature, Storage	-40 to 125 C
	Humidity, non-condensing	<40C 0-90%, >40C 0-75%

Various Configurations of the LS-48-M Series
Rackmount, Portable and Modular

1U 12" Chassis

1U 22" Deep Chassis

2U 12" Chassis

Desktop Chassis

Pelican 1450 Chassis

**Lumistar DPE Delivery Options
(LS-68-M or LS-48-M)**

Typical GUI for the LS-48-M Series Products

PCM Output Encoder Selections

NRZ-L	Non Return To Zero - Level
NRZ-M	Non Return To Zero - Mark
NRZ-S	Non Return To Zero - Space
RNRZ11-L	PRN11 Randomized Non Return To Zero - Level
RNRZ11-M	PRN11 Randomized Non Return To Zero - Mark
RNRZ11-S	PRN11 Randomized Non Return To Zero - Space
RNRZ15-L	PRN15 Randomized Non Return To Zero - Level
RNRZ15-M	PRN15 Randomized Non Return To Zero - Mark
RNRZ15-S	PRN15 Randomized Non Return To Zero - Space
RNRZ17-L	PRN17 Randomized Non Return To Zero - Level
RNRZ17-M	PRN17 Randomized Non Return To Zero - Mark
RNRZ17-S	PRN17 Randomized Non Return To Zero - Space
RNRZ23-L	PRN23 Randomized Non Return To Zero - Level
RNRZ23-M	PRN23 Randomized Non Return To Zero - Mark
RNRZ23-S	PRN23 Randomized Non Return To Zero - Space
BIO-L	Bi Phase - Level
BIO-M	Bi Phase - Mark
BIO-S	Bi Phase - Space
RZ	Return To Zero
DM-M	Delay Modulation (Miller Code) - Mark
DM-S	Delay Modulation (Miller Code) - Space
DBIO-M	Differential Bi Phase - Mark
DBIO-S	Differential Bi Phase - Space
MDM-M	Modified Delay Modulation (Miller Code) - Mark
MDM-S	Modified Delay Modulation (Miller Code) - Space

Clock Phase Relationships