What is FPGA Zynq UltraScale+ with MPSoC?

Bulletin # 8401065

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Introduction

This paper is a brief overview of some of Acromag's APZU FPGA Zynq® UltraScale+™ with MPSoC products, as well as the features of AcroPack Zynq UltraScale+, the carrier boards that host AcroPack mezzanine modules. We'll highlight some of the development tools, the engineering design kit, and the software available. In addition, we'll discuss some applications and give you an overview of the FPGA products that Acromag supports in the Xilinx offerings.

Types of FPGA Zynq UltraScale+ with MPSoC

Acromag's FPGA Zynq UltraScale+ with MPSoC (MultiProcessor System on a Chip) has three series: the CG series, the EG series, and lastly the EV series. This paper will be focused on the CG series. Acromag uses the XCZU3CG in our product in a 484-pin package (XCZU3CG-2SBVA484I).

CG Series

The Zynq CG series has a Dual-Core Cortex-A53 (APU) application processor. In addition to that comes a Neon media processing engine and a Dual-Core Cortex R5 (RPU), which is a real-time processing unit.

EG Series

The EG family has the same set of features of the CG, however it uses a Quad-Core Cortex-A53 and includes a graphics processing unit (GPU) based on the Mali-400MP2. Acromag products are primarily going to be CG, but there is a possibility to do a PIN-compatible EG with the AcroPack Zynq UltraScale+.

EV Series

Similarly, the Zynq EV family has the same features as the EG: Quad-Core Cortex-A53 and GPU. However, it adds a video codec that can do H.264 and H.265.

Features of AcroPack Zynq UltraScale+

Feature	Zynq CG	Zynq EG	Zynq EV
Dual-Core Cortex-A53 (APU)	X		
Neon (Media Processing Engine)	X	X	X
Dual-Core Cortex R5 (RPU)	X	X	X
Quad-Core Cortex-A53		X	X
Graphics Processing Unit		X	X
Video Codec			X

Table 1: Features of AcroPack Zynq UltraScale+

APZU Carrier Boards

The graphic below shows the APZU-30x. Acromag is introducing three I/O versions; the APZU-301, APZU-A303, and APZU-304.

There are two parts of the Zynq UltraScale+ chip:

1. The Processing System (where the multi-processor ARM, Real-time processor and GPU are located)

The Programmable Logic (PL) side (where the reconfigurable logic is located).

APZU30x Block Diagram

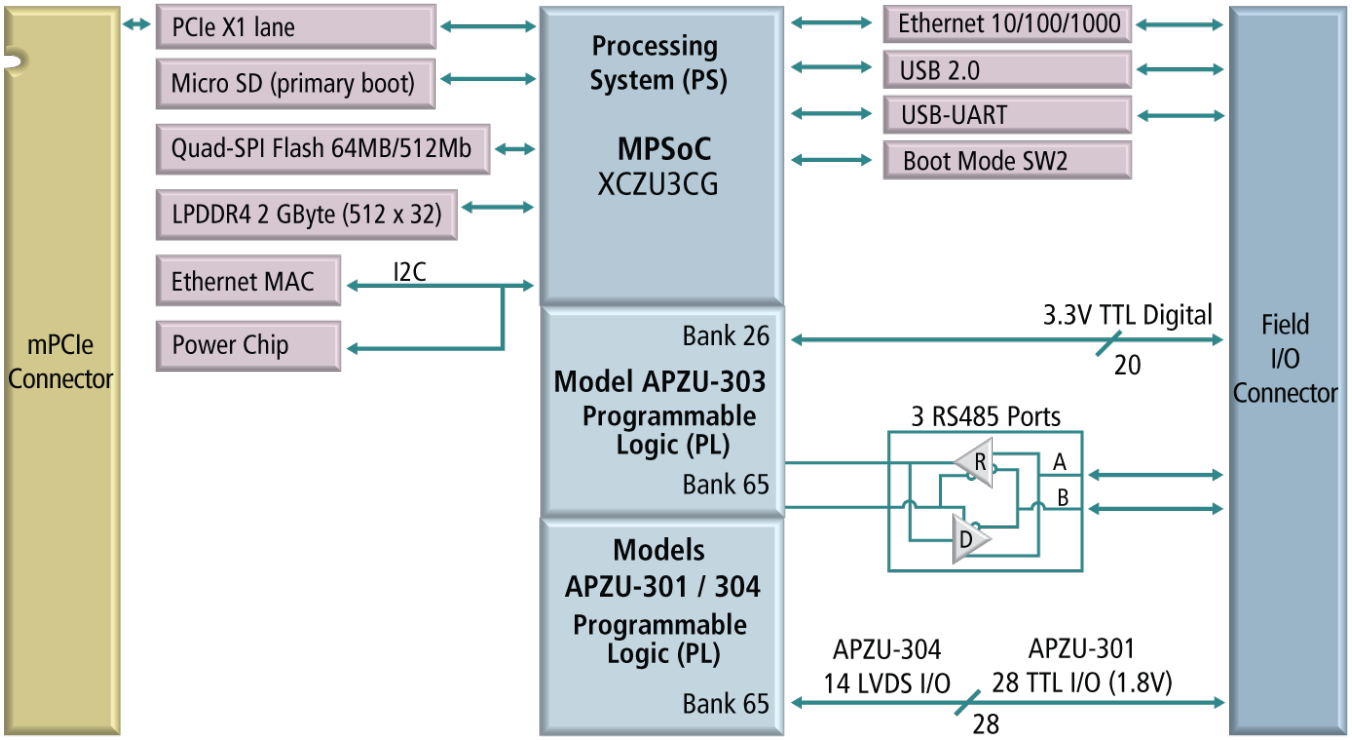


Figure 1: APZU Block Diagram

As shown above, we are bringing out an Ethernet that's 10/100/1000 compatible to the field I/O, a USB 2.0 port, a USB to UART, and a power switch along with a reset switch; these are common amongst all three models.

The I/O is different, however, the APZU-301 will have 28 TTL; the -303 will be a combination of 20 TTL and three R-485/422 serial channels; and the -304 will be 14 low-voltage differential signaling channels.

APZU FPGA Mezzanine Module

There's also an APZU breakout panel. It's basically a printed circuit board and has the magnetics on it for the Ethernet so you can connect an RJ45 cable. It has a USB 2.0 connector and a USB to UART COMs port, as well as the digital I/O available on this breakout panel. (More detail about that later.)

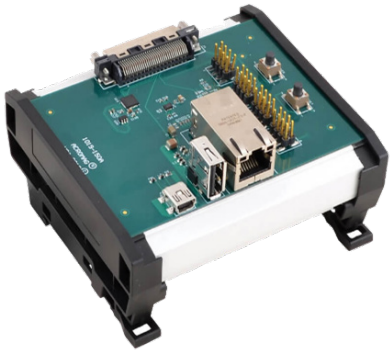


Figure 2: Breakout Panel

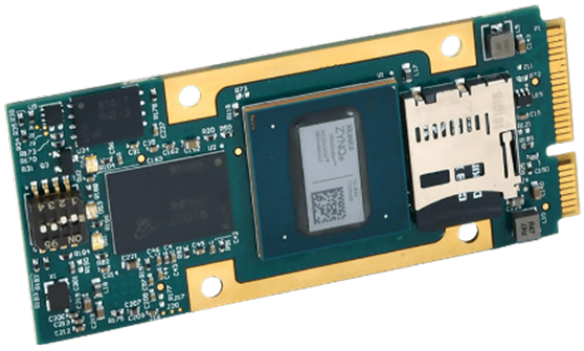


Figure 3: AcroPack APZU

The primary boot for the processors is through a micro SD secure digital card and as can be seen in the picture of the AcroPack (Figure 3), we've got a socket where the micro SD will plug into. There's also another boot option in case you want to boot through the quad SPI flash. So, you'll have the ability to load your OS either through the micro SD or the Quad SPI flash. Further, there's 2 Gbytes of low power DDR4 DRAM on the board, and that's organized as a 512Mbit x 32.

FPGA Zynq UltraScale+ MPSoC Processors CG

The processors in the CG family as mentioned earlier, are dual-core ARM Cortex A53; this is ARM 8-like. It operates up to 1.3 GHz and it is a 64-bit data and 64-bit instruction. Within that processing unit, there's a NEON processor, which we will go into more detail about later.

There's also the dual-core ARM Cortex R5, the real-time processor. This operates up to 533 MHz and is a 32-bit architecture, with hardware-floating point.

Dual Core ARM Cortex-A53

Up to 1.5GHz Operation

Harvard Architecture

- 64-bit Data
- 64-bit Instruction

NEON Processor

Dual Core ARM Cortex R5

Up to 600 MHz Operation

32-bit Architecture

Hardware Floating-point Unit

Real-time Processor

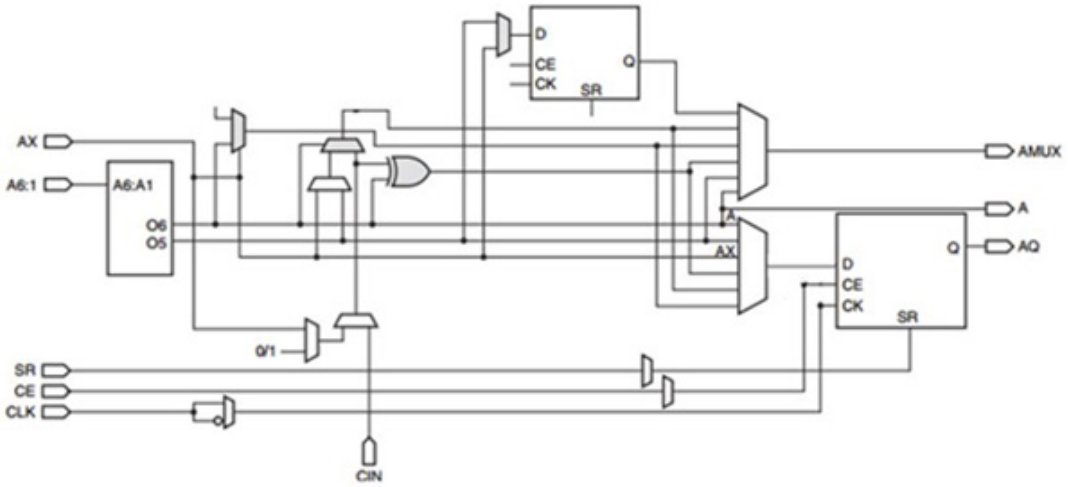
Media-Processing Engine: NEON Processor

The media-processing engine called a NEON is a hardware accelerator. It's part of the application processing unit, and is an advanced single-instruction, multiple-data architecture. Basically, it allows you to accelerate audio and video encoding and decoding and accelerates signal processing algorithms.

FPGA Logic Cell

The graphic below is an example of an FPGA logic cell. It's identified as a 6-input Look Up Table or LUT (also commonly referred to as a function generator), and the logic cell.

6-input LUT and the Logic Cell




```
process (CK, SR)
begin
    if (SR = '1') then
       AQ <= '0';
    elsif rising_edge(CK) then
       AQ <= ( WriteStb and AXI_d0 and valid) or (AQ and not WriteStb);
    end if;
end process;
```

Figure 4: Example of an FPGA logic cell

This is shown so you can understand the ability to take a configurable logic block and each one of these configurable logic blocks has eight of these LUTs and 16 flip-flops. So, you'll be able to reconfigure anyway that you want to interconnect the logic blocks, as well as being able to reprogram them, per your performance requirements.

How is FPGA Device Capacity Measured?

As an illustration, the table below shows the ZU3CG, which is our primary AcroPack Zynq UltraScale+ device, and how it compares to the Artix 7A50T, an Artix 7A200T, and a Kintex 7K325T.

How to Measure Device Capacity

	ZU3CG	XC7A50T	XC7A200T	XC7K325T
Logic Cells	154,350	52,160	215,360	326,080
6-Input Lut	70,560	32,600	134,600	203,800
4-Input LUT Radio Scaling Factor	2.1875	1.6	1.6	1.6
Logic Cell = 4-Input LUT Calculation	70,560 x 2.1875 = 154,350	32,600 x 1.6 = 52,160	134,000 x 1.6 = 215,360	203,800 x 1.6 = 326,080

Table 2: Device Capacity

Initially, Xilinx Virtex 4 devices were 4-input LUT / function generators, and the logic cell was said to be equal to a 4-input Look Up Table (LUT) in one flip flop. Therefore, Xilinx still measures the size of their FPGA in terms of 4-input function generators. However, things changed with the introduction of the Virtex 5 family, when the logic cell became a 6-input LUT. So, Xilinx came up with the ratio that a 6-input LUT was 1.6 times a 4-input LUT. Therefore, you were able to come up with an equivalent amount of logic cells, to be able to measure sizes of the different FPGAs.

Acromag offers the AcroPack 7A50T version (APA7-501, -502, -503 and -504), and it has approximately 52,160 logic cells. In contrast, the Zynq UltraScale+ has much more functionality and more resources available. As a result, Xilinx came up with a ratio scaling factor of 2.1875. There's approximately 70,560 6-input LUTS on this 3CG product. When you do the math, that comes out to 154,000 logic cells. As shown above, that's roughly about three times the size of a 7A50T, in terms of logic cells on the 3CG board.

Processor Memory

Processor memory is comprised of 32KB L1 caches, both instruction and data. It has 1MB of a unified L2 cache, which is shared between the processors, and dual-core or quad-core will share that memory. Additionally, there's a 32-bit interface to the 2GB of LPDDR4 main memory.

Working with the Zynq UltraScale+, you will boot up the processor system first, then when you configure the programmable logic, that control will be done by the processing system.

32KB L1 Caches

Fastest (specific to processor)

1MB Unified L2 Cache

2GB LPDDR4 Main Memory

32-bit Data Width

Faster & Shared Between Processors

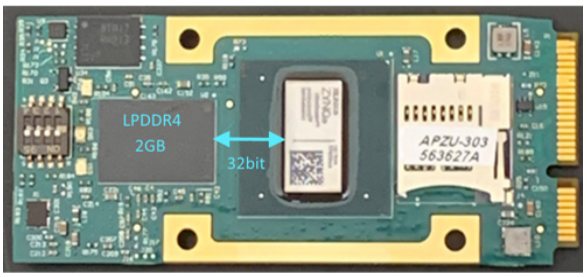


Figure 5: Zynq chip has 32-bit interfaces to LPDDR4 memory

PCIe Interface

All the AcroPacks, including the Zynq UltraScale+, include a x1 Gen. 1 PCI Express link to the module over the front finger connector, which is 2.5GB per second. With the Zynq, the x1 link is to the PS-GTR. APZU MPSoCs include integrated blocks for PCIe that are compliant PCI Express Base Specification Revision 3.1. There are also two general-purpose DMA controllers on the Zynq UltraScale+.

APZU Include PCIe

x1 at Gen. 1 Rates

2 General-purpose DMA Controllers

Compliant PCIe Base Specification Revision 3.1

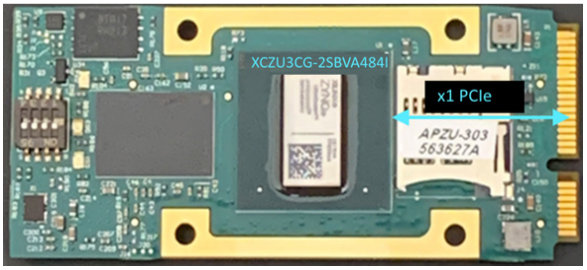


Figure 6: All AcroPacks include a x1 Gen1 PCIe link

APZU I/O Peripherals

Triple-Speed Gigabit Ethernet

The Zynq UltraScale+ Processing System (PS) is equipped with four 10/100/1000 Ethernet controllers. We use one for a Gigabit Ethernet connection.

Due to the limitation of the I/O, we are just going to be bringing out one 10/100/1000 Ethernet channel. This will use a Reduced Gigabit Media Independent Interface (RGMII), and as can be seen in the picture to the right, there's a small breakout board, the 5028-626.

You can see a 68-pin cable connected to the carrier on the upper right side of the photo. This cable is one foot in length and goes to the printed circuit board below. The Ethernet magnetics are on that board, allowing you to have a copper RJ45 port. Additionally, you can see a USB 2.0 port, as well as a USB to UART com port, available.

There are two buttons down at the bottom of the printed circuit board; one for power, and one for reset. And you can see all the digital I/O that are coming out of the Zynq UltraScale+; whether TTL, low voltage differential, or the combination at those jumpers, there are four jumpers down there.

This is a development board that we recommend customers use to get started with. However, each application will dictate what a customer will go to production with.

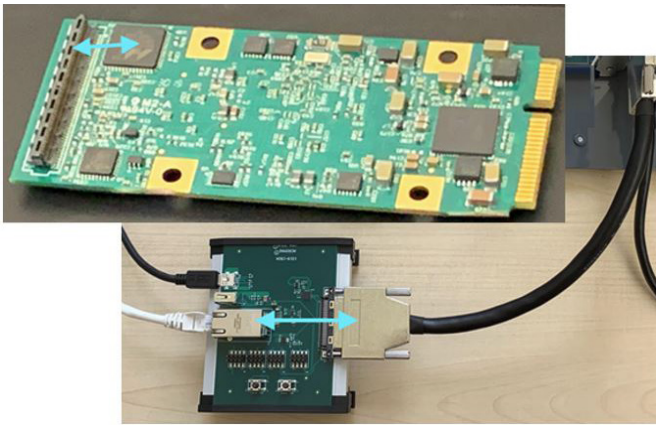


Figure 7: Acromag APZU with breakout board 5028-626

SD Controller

As was noted earlier, there is a secure digital interface, and this is the primary boot. It's a 16GB micro SD. That is the primary boot and it's included in the shipment of the product. This will allow users to load PetaLinux and/or any other operating system that they may need.

In addition, there is a secondary boot option with a flash device, which is much smaller. So, users can do development using a micro SD flash card and then once the code is optimized, they can boot from the Quad Flash device.

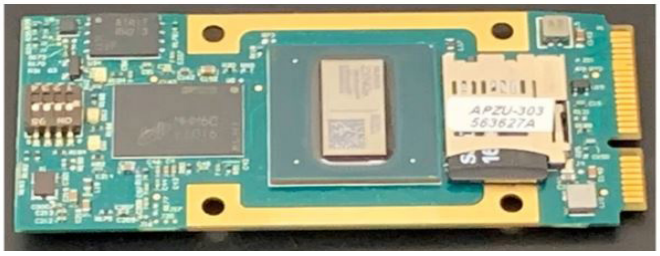


Figure 8: APZU with 16GB micro SD

I2C

Acromag uses I2C ("I squared C"), we communicate with a 2K EEPROM for the Ethernet Mac ID and for the power chip. That monitors voltages and temperatures on the board as well as on the chip, making sure that things stay within specifications.

SWaP Optimized

As can be seen to the right: a picture of the AcroPack Zynq UltraScale+, with the heat spreader included. Power dissipation with approximately 80% of the resources used will be less than 5 watts.

Size = 70mm x 30mm

Weight = 35.18 g (including heat spreader)

Figure 9: APZU with heat spreader

APZU PCIe Carriers

APCe7012

The APCe7012 supports one AcroPack, and is a x1 Edge connector interface. In addition, it's a small, half-height card that can host other AcroPack modules that use isolated DC-to-DC modules for power.

Supports 1 AcroPack

Supports Analog Isolated Modules

Available in Half-height

68-pin 0.8mm Connector

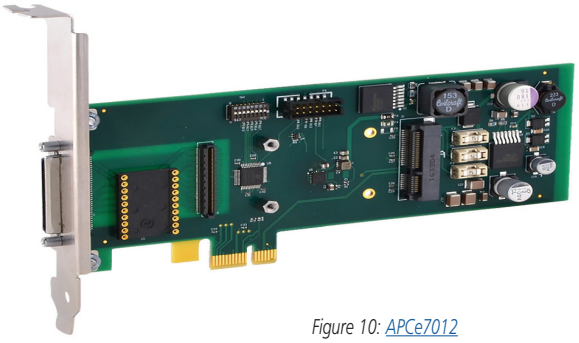


Figure 10: APCe7012

APCe7022

Comparatively, the APCe7022 is a dual AcroPack carrier and is a x4 Edge connector interface. The APCe7022 can also host other AcroPack modules. Additionally, all Acromag carriers have been developed to be able to host Mini PCI Express cards.

Supports 2 AcroPacks

Two 68-pin 0.8mm Connectors

PCIe x4 Edge Connector

Figure 11: APCe7022

APCe7040 & APCe7043

Acromag has two quad carrier boards for PCI Express servers: a full-length carrier, the APCe7040, as well as a 3/4-length carrier, the APCe7043. The APCe is the full-length version of the quad, as can be seen in the photo on the right. These can host analog isolated modules, in addition to up to four AcroPacks or combination of AcroPacks and Mini PCI Express cards.

To summarize, both versions:

Support 4 AcroPacks

Support Analog Isolated Modules

68-pin 0.8mm Connector

PCIe x4 Edge Connector

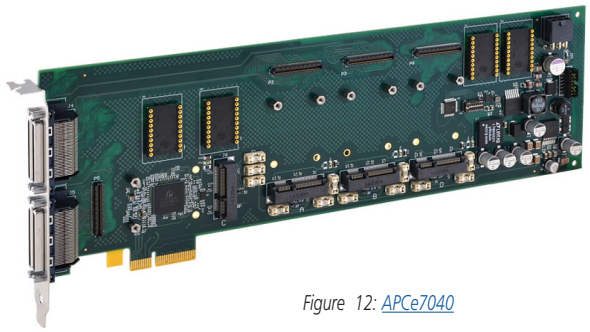


Figure 12: APCe7040

More AcroPack Carriers for APZU

XMC AcroPack Carrier

The XMCAP2020 is Acromag's front I/O XMC AcroPack carrier, while the XMCAP2021 is a rear I/O version, and the XMCAP2022 is a carrier that's used in the ARCX4000 box to host two AcroPacks.

In addition, Acromag offers two 6U VPX carriers. The VPX4520 has an expansion plane interface, while the VPX4521 has a data plane interface to the backplane. Each of these supports up to four AcroPack modules and one XMC card that can be either a Vita 42 or Vita 61 configuration. Each of these supports up to four AcroPack modules and one XMC card that can be either a VITA 42 or VITA 61 configuration. They are available in either front I/O air-cooled or rear I/O conduction-cooled versions.

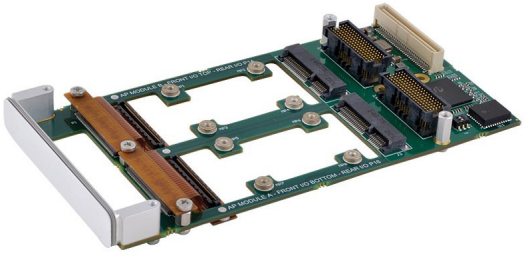


Figure 13: XMCAP2021

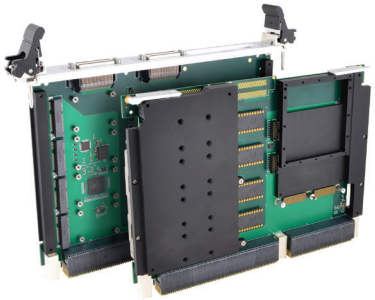


Figure 14: VPX4520 and VPX4521

ACEX4041 Carrier & ARCX1100

The ACEX4041 carrier hosts four AcroPack modules as well as an M.2 storage and requires a Type 10 Com Express processor. We then took this carrier, and introduced the ARCX1100, which packages the ACEX-4041 in an IP65 chassis and has a removable 2.5 inch solid state drive.

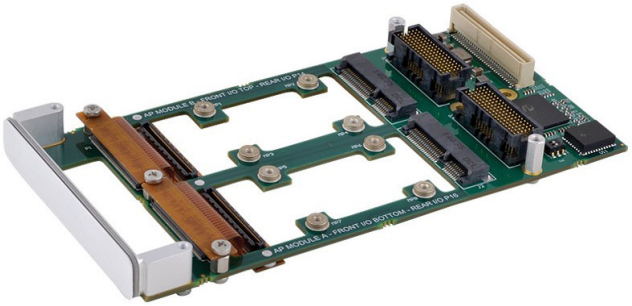


Figure 15: ACEX4041 carrier with 4 AcroPacks

Figure 16: ARCX1100

ACPS3310/20 Compact PCIe Serial

AcroPacks also support Compact PCI Express serial. There are two versions, both of which host two AcroPack modules and support isolated analog I/O: the ACPS3310 supports front I/O, while the ACPS3320 supports rear I/O.

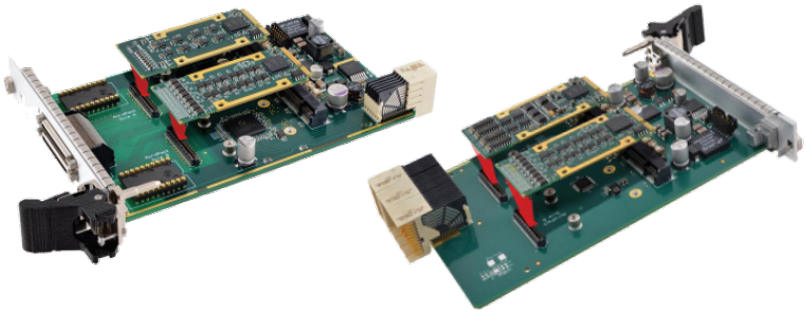


Figure 17: ACPS3310 (left) & ACPS3320 (right) Compact PCIe Serial

EDK, Software Drivers & Development Tools

Engineering Design Kit (EDK)

At first purchase, the Engineering Design Kit, APZU-EDK, that Acromag offers is a must-buy. It provides example code of intellectual property blocks, as well as the RAM, system monitors, and AXI interfaces to the digital I/O. It's "known good code" that users can import into their Vitis development environment, knowing that this code has been debugged, and thus, works. The EDK is a starting point for users to add to their application, then start making modifications. Accordingly, this is a one-time purchase.

Software Support

APSW-API-LNX: Support for Linux; free website download (see the software tab on the link)

APSW-API-WIN: Support for Windows/DLL drivers

APSW-API-VXW: Support for VxWorks 7.0

I/O Breakout Panel

The 5028-626 I/O breakout panel is also recommended, it has a 68-pin, male-to-male cable that's one foot long and one side of it plugs into the carrier front panel. The other side plugs into the breakout panel, thus bringing an Ethernet port, UART to USB port, digital I/O at the jumper blocks and power and reset buttons out to the field.

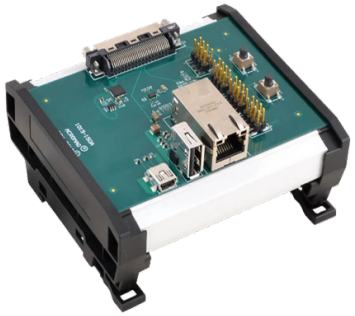


Figure 18: I/O Breakout Panel

Development Tools

Vivado® 2020.1 Design Suite – Vitis™

Vitis is a unified software platform that sits on top of Vivado and allows you to do your development on a variety of different Xilinx platforms, including the Systems on a Chip (SoCs) as well as the Versal ACAPs. The Vitis software provides compilers, analyzers, and debuggers so users can design, develop software, and develop code.

PetaLinux

Correspondingly, PetaLinux is an embedded Linux systems development kit that targets Xilinx SoCs designs. It includes U-Boot, Linux Kernel, and Device Tree, as well as Root Filesystem components.

APZU Applications

Typical applications for the AcroPack Zynq UltraScale+ include:

Hardware in the Loop

Firstly, hardware in the loop used for simulation is a key application for these modules.

Protocol Converter

With the processing, memory, and algorithms available, users can go from one type of format to another with their protocol converters.

Video Capture & Recording

Interfaces such as camera link, USB, and Ethernet make the APZU very capable for video capture and recording.

Video Packet Interrogation

The APZU is very beneficial for applications such as facial recognition or license plate numbers, etc.

Missile Simulation

The ability to simulate not only a missile, but other types of weapons, makes these modules ideal.

Sensor Data Acquisition

The APZU can take a variety of different sensor data acquisition, then process them, transmit them along, etc.

FPGA Product Lines Supported

Without a doubt, Acromag is very strongly partnered with Xilinx. We currently support the Virtex-4, the Virtex-5, Spartan-6, Kintex-7, and the Artix-7 (in both an XMC form factor and in an AcroPack form factor). Furthermore, with the development of the new Zynq UltraScale+, we'll be supporting the APZU-30x family. Coming soon, we will have an XMC Zynq UltraScale+ offering.

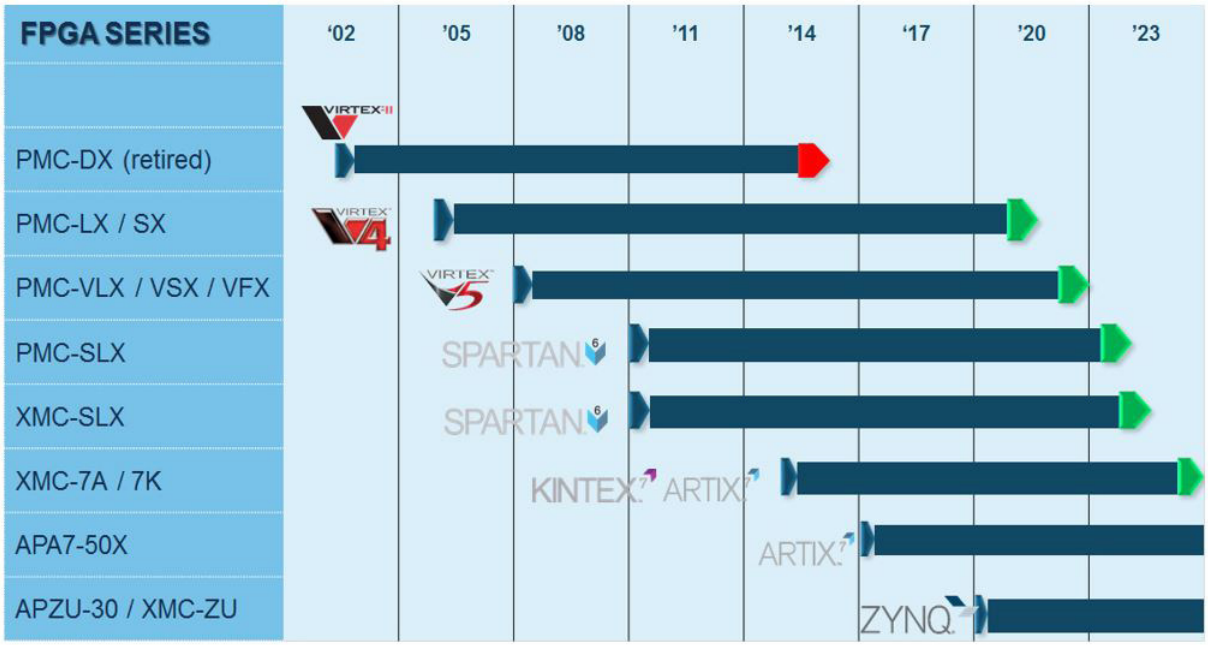


Table 3: Acromag FPGA Product Lines

About Acromag

Founded in 1957, Acromag, Inc. designs and manufactures high-tech electronics. They are an international corporation headquartered near Detroit, Michigan with a global network of sales representatives and distributors. Acromag offers a complete line of embedded computing and I/O solutions including general purpose I/O boards, single-board computers, FPGA modules, embedded computers, COM Express products, mezzanine modules, wiring accessories, and software. Industries served include military, aerospace, manufacturing, transportation, utilities, and scientific research laboratories.

For more information about FPGAs, Zynq UltraScale+, or any Acromag product, call Inside Sales at (248) 295-0310 or Marketing Communications at (248) 295-0866. Or visit our website: www.acromag.com.

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How to Reduce Costs with Customized I/O on COTS FPGA Modules

What are PMC and XMC Modular I/O Standards?

How to Use FPGAs for Speed & Flexibility

How do FPGA Modules Drive Real-Time Applications?

How to Install an XMC-7K325AX-LF FPGA Module with an AXM-D02 or AXM-A75 I/O Module, Installed on an Apce8675 Carrier Card

How Does Conduction Cooling Keep Heat in Check?

Click here to watch the full FPGA Zynq UltraScale+ MPSoC Introduction Webcast

What is FPGA Zynq UltraScale+ with MPSoC?